Listing of Claims:

1. (previously presented) A radio interface for interfacing an analog radio module to a digital module, the interface comprising:

a serial bus processor,

a programmable radio interface processor (RIP) that includes at least one memory-mapped register configured to control data generated by the serial bus processor; and

a plurality of lookup tables which are indexed by data received from the analog radio module, and which are programmed with data so as to compensate for one or more nonlinearities which may be present in the analog radio module, but are not accounted for in the digital module;

wherein the serial bus processor receives data from the plurality of lookup tables, and uses data values retrieved from the lookup tables to generate processed data for controlling the digital module.

2. (canceled)

3. (original) The radio interface of claim 1 wherein the RIP includes a finite state machine equipped to access the memory-mapped registers, and wherein

the memory-mapped registers are used to control the processed data generated by the serial bus processor.

4. (original) The radio interface of claim 3 further including a processor interface for accessing the memory-mapped registers.

5. (original) The radio interface of claim 3 further including one or more general-purpose Input/Output (GPIO) registers for accessing the memory-mapped registers.

6. (original) The radio interface of claim 1 further comprising a clock, coupled to the RIP, for determining the relative timing of external events, and also for controlling the analog radio module.

7. (previously presented) The radio interface of claim 1 wherein the serial bus processor is configured to control at least one of IBus, PBus or RBus.

8. (original) The radio interface of claim 1 wherein the RIP translates high-level commands received from the digital module, specifying at least one of gain settings and power measurements, into low-level commands which are sent to

the analog radio module, thereby eliminating generation of analog-specific command sequences in the digital module.

9. (original) The radio interface of claim 1 wherein the RIP accesses controlling software that is programmed according to one or more specific electronic characteristics of a given analog radio module.

10. (original) The radio interface of claim 1 wherein the nonlinearities include at least one of AGC (automatic gain control) line voltage as a function of gain, and power level control voltage as a function of power output, whereby the digital module need not be modified to work with the specific characteristics of a given analog radio module.

11. (original) The radio interface of claim 1 wherein the digital module is a time-division-duplex, user-equipment, application-specific-integrated-circuit (TDD UE ASIC), thereby permitting the TDD UE ASIC to be utilized in conjunction with any of a plurality of analog radio modules without redesigning the analog radio module or the ASIC.

12. (previously presented) A method for interfacing an analog radio module to a digital module in a system that comprises (i) a serial bus processor, (ii) a programmable radio interface processor (RIP) that includes one or more memory-mapped registers coupled to the serial bus processor, and (ii) a plurality of lookup tables; the method comprising:

programming the plurality of lookup tables with data so as to compensate for one or more nonlinearities which may be present in the analog radio module, but are not accounted for in the digital module;

indexing the plurality of lookup tables using data received from the analog radio module;

the serial bus processor receiving data from the plurality of lookup tables, and

the serial bus processor using data values retrieved from the lookup tables to generate processed data for controlling the digital module; and

controlling the processed data using the memory mapped registers.

13. (canceled)

14. (previously presented) The method of claim 12 further including providing the RIP with a finite state machine equipped to access the memory-

mapped registers, and using the memory-mapped registers to control the processed data generated by the serial bus processor.

15. (previously presented) The method of claim 14 further including accessing the memory-mapped registers using a processor interface.

16. (previously presented) The method of claim 14 further including using one or more general-purpose Input/Output (GPIO) registers for accessing the memory-mapped registers.

17. (previously presented) The method of claim 12 further including using a clock, coupled to the RIP, for determining the relative timing of external events, and also for controlling the analog radio module.

18. (previously presented) The method of claim 12 wherein the serial bus processor is configured to control at least one of IBus, PBus or RBus.

19. (previously presented) The method of claim 12 further including the RIP translating high-level commands received from the digital module, which specify at least one of gain settings and power measurements, into low-level

commands, and sending the translated low-level commands to the analog radio module, thereby eliminating generation of analog-specific command sequences in the digital module.

20. (previously presented) The method of claim 12 further including the RIP executing controlling software that is programmed according to one or more specific electronic characteristics of a given analog radio module.

21. (original) The method of claim 12 wherein the nonlinearities include at least one of AGC (automatic gain control) line voltage as a function of gain, and power level control voltage as a function of power output, whereby the digital module need not be modified to work with the specific characteristics of a given analog radio module.

22. (original) The method of claim 12 wherein the digital module is a time- division-duplex, user-equipment, application-specific-integrated-circuit (TDD UE ASIC), thereby permitting the TDD UE ASIC to be utilized in conjunction with any of a plurality of analog radio modules without redesigning the analog radio module or the ASIC.

23. (previously presented) A radio interface for interfacing between an analog radio module and a digital module, the interface comprising:

a serial bus processor,

a programmable radio interface processor (RIP); and

a plurality of lookup tables indexed by data received from the analog radio module wherein data values retrieved from the lookup tables may be used to generate processed data for controlling the digital module and the RIP includes at least one memory-mapped register coupled to the serial bus processor.

24. (canceled)

25. (original) The radio interface of claim 23 wherein the plurality of lookup tables are programmed with data so as to compensate for one or more nonlinearities which may be present in the analog radio module, but are not accounted for in the digital module.

26. (original) The radio interface of claim 23 wherein the serial bus processor receives data from the plurality of lookup tables, and uses data values retrieved from the lookup tables to generate processed data for controlling the digital module.

27. (previously presented) The radio interface of claim 23 wherein the memory-mapped registers are used to control the processed data generated by the serial bus processor.

28. (original) The radio interface of claim 23 wherein the RIP includes a finite state machine equipped to access memory-mapped registers, and wherein the memory-mapped registers are used to control the processed data generated by the serial bus processor.

29. (original) The radio interface of claim 28 further including a processor interface for accessing the memory-mapped registers.

30. (original) The radio interface of claim 28 further including one or more general-purpose Input/Output (GPIO) registers for accessing the memory-mapped registers.

31. (original) The radio interface of claim 23 further comprising a clock, coupled to the RIP, for determining the relative timing of external events, and also for controlling the analog radio module.

32. (previously presented) The radio interface of claim 23 wherein the serial bus processor is configured to control at least one of IBus, PBus or RBus.

33. (original) The radio interface of claim 23 wherein the RIP translates high-level commands received from the digital module, specifying at least one of gain settings and power measurements, into low-level commands which are sent to the analog radio module, thereby eliminating generation of analog-specific command sequences in the digital module.

34. (original) The radio interface of claim 23 wherein the RIP accesses controlling software that is programmed according to one or more specific electronic characteristics of a given analog radio module.

35. (original) The radio interface of claim 23 wherein the nonlinearities include at least one of AGC (automatic gain control) line voltage as a function of gain, and power level control voltage as a function of power output, whereby the digital module need not be modified to work with the specific characteristics of a given analog radio module.

36. (original) The radio interface of claim 23 wherein the digital module is a time- division-duplex, user-equipment, application-specific-integrated-circuit (TDD UE ASIC), thereby permitting the TDD UE ASIC to be utilized in conjunction with any of a plurality of analog radio modules without redesigning the analog radio module or the ASIC.